CLAIMS

What is claimed is:

1. A system, comprising:

a timing logic unit coupled to produce a predetermined number of pulses in response to a transaction request transmitted from a source device to a target device, wherein the timing logic unit is configured to generate a time expired signal upon producing a last one of the predetermined number of pulses; and

a processor for executing program instructions configured to programmably alter a rate at which the predetermined number of pulses are produced by the timing logic unit, thereby adjusting an expiration period for completing a transaction cycle associated with the transaction request.

2. The system as recited in claim 1, wherein the program instructions are configured to programmably decrease the rate for increasing the expiration period.

3. The system as recited in claim 1, wherein the program instructions are configured to programmably increase the rate for decreasing the expiration period.

4. The system as recited in claim 1, wherein the timing logic unit is arranged within at least one of the source and target devices.

5. The system as recited in claim 4, further comprising a carrier medium configured to transfer information associated with the transaction cycle between the source device and the target device.

6. The system as recited in claim 5, wherein the carrier medium comprises one or more buses within a computer system, such that the source and target devices are each arranged within the computer system.

7. The system as recited in claim 5, wherein the carrier medium comprises a wired or wireless network interface for coupling the system to one or more additional systems, such that the source device is arranged within the system and the target device is arranged within one of the additional systems, or vice versa.

8. A computer system, comprising:

a source device configured to initiate a transaction cycle by sending a transaction request to a target device;

a timing logic unit arranged within the target device, wherein the timing logic unit comprises:

a time register for storing a predetermined expiration value;

a first counter for receiving a number of pulses corresponding to the predetermined expiration value, and generating a time expired signal upon receipt of a last one of the number of pulses; and

a memory device for storing program instructions configured to programmably alter a rate at which the number of pulses are received by the first counter, thereby adjusting an expiration period for completing the transaction cycle.

9. The computer system as recited in claim 8, wherein the program instructions are configured to programmably decrease the rate, thereby increasing the expiration period, if a target-ready signal is not asserted by the target device before the time expired signal is generated by the timing logic unit.

10. The computer system as recited in claim 8, wherein the program instructions are configured to programmably increase the rate, thereby decreasing the expiration period, if a target-ready signal and a source-ready signal are asserted by the target device and the source device, respectively, before the time expired signal is generated by the timing logic unit.

11. The computer system as recited in claim 9, wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle.

12. The computer system as recited in claim 10, wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle.

13. The computer system as recited in claim 8, further comprising a processor coupled for receiving interrupt signals from a clock source at a fixed rate and for executing the program instructions in response to the interrupt signals.

14. The computer system as recited in claim 13, wherein the timing logic unit further comprises:

a control register for storing an enable signal;

a second counter for generating the number of pulses; and

a circuit comprising the time register and the first counter, wherein the circuit is coupled to receive the enable signal and at least one of the number of pulses every $n^{th}$ time the processor receives an interrupt signal, wherein 'n' is a programmable value selected from a group consisting of any positive, non-zero integer value.

15. The computer system as recited in claim 14, further comprising a primary bus bridge logic unit configured to coordinate transactions between the processor, the memory device, and one or more peripheral devices coupled to the primary bus bridge logic unit over one or more peripheral buses of the computer system.

16. The computer system as recited in claim 15, wherein the timing logic unit is arranged within the primary bus bridge logic unit.

17. The computer system as recited in claim 15, wherein the timing logic unit is arranged within the one or more peripheral devices.

18. The computer system as recited in claim 15, further comprising a secondary bus bridge unit coupled to the primary bus bridge unit over one of the peripheral buses and having one or more additional peripheral devices coupled thereto, wherein the timing logic unit is arranged within the secondary bus bridge unit and/or within the one or more additional peripheral devices.

19. A method for adjusting an expiration period for completing a transaction cycle conducted between source and target devices within a system, the method comprising:

extending the expiration period to allow the transaction cycle to be completed, wherein said extending comprises:

receiving interrupt signals at a processor of the system, wherein the interrupt signals are generated at a fixed rate by a clock source of the system; and

altering a pulse rate of a timing logic unit of the system by enabling the timing logic unit to generate a pulse every $n^{th}$ time the processor receives an interrupt signal, wherein 'n' is a programmable value selected from a group consisting of any positive, non-zero integer value.

20. The method as recited in claim 19, wherein said altering extends the expiration period by producing a predetermined number of pulses at a programmable rate, which is slower than the fixed rate by a factor of 1/n.

21. The method as recited in claim 20, wherein said altering a pulse rate comprises:

receiving a first bit pattern from the processor to place the timing logic unit into a 'no pulse' state;

receiving a first control bit from the processor to place the timing logic unit into an 'enable' state;

receiving a second bit pattern, which differs from the first bit pattern, from the processor to place the timing logic unit into a 'pulse' state; and

receiving a second control bit, which differs from the first control bit, from the processor to place the timing logic unit into a 'disable' state.

22. The method as recited in claim 21, wherein the steps associated with said altering a pulse rate are repeated a number of times equal to the predetermined number.

23. The method as recited in claim 19, further comprising:

reducing the expiration period, wherein said reducing comprises:

receiving interrupt signals at the processor, wherein the interrupt signals are generated at the fixed rate by the clock source; and

altering a pulse rate of the timing logic unit by enabling the timing logic unit to generate 'm' number of pulses every $n^{th}$ time the processor receives an interrupt signal, wherein 'm' and 'n' are programmable values selected from a group consisting of any positive, non-zero integer value.

24. The method as recited in claim 23, wherein 'm' is selected from a group consisting of any positive, non-zero integer value less than the predetermined number, and wherein 'n' is selected from a group consisting of any positive, non-zero integer value less than 'm'.

25. The method as recited in claim 24, wherein said altering reduces the expiration period by producing a predetermined number of pulses at a programmable rate, which is faster than the fixed rate by a factor of m/n.

26. The method as recited in claim 25, wherein said altering a pulse rate comprises:

receiving a first bit pattern from the processor to place the timing logic unit into a 'no pulse' state;

receiving a first control bit from the processor to place the timing logic unit into an 'enable' state;

receiving a plurality of second bit patterns, each different from the first bit pattern, from the processor to place the timing logic unit into a 'pulse' state multiple times; and

receiving a second control bit, different from the first control bit, from the processor to place the timing logic unit into a 'disable' state.

27. The method of claim 26, wherein the steps associated with said altering a pulse rate are repeated a number of times equal to the predetermined number divided by 'm'.

28. A computer-usable carrier medium, comprising:

first program instructions executable on a computer system for enabling a timing logic unit of the computer system to generate one or more pulses;

second program instructions executable on the computer system for repeating the first program instructions upon receiving every $n^{th}$ interrupt signal at a processor of the computer system, wherein 'n' is a programmable value selected from a group consisting of any positive, non-zero integer value, and wherein execution of the second program instructions cause the timing logic unit to generate a time expired signal.

29. The computer-usable carrier medium as recited in claim 28, wherein execution of the second program instructions increases or decreases an expiration period for completing a transaction cycle conducted between source and target devices coupled within or to the computer system.

30. The computer-usable carrier medium as recited in claim 29, wherein the expiration period is decreased by enabling the timing logic unit to generate more than one pulse for every $n^{th}$ interrupt signal received by the processor.

31. The computer-usable carrier medium as recited in claim 29, wherein the expiration period is increased by enabling the timing logic unit to generate one pulse for every $n^{th}$ interrupt signal received by the processor.

32. The computer-usable carrier medium as recited in claim 29, wherein the first program instructions are adapted to:

initialize the timing logic unit by generating a first bit pattern in a second counter of the timing logic unit;

enable the timing logic unit by setting one or more bits in a control register of the timing logic unit to a first logic level;

generate the one or more pulses by consecutively generating one or more second bit patterns, different from the first bit pattern, in the second counter of the timing logic unit; and

33. The computer-usable carrier medium as recited in claim 32, wherein the second program instructions are adapted to:

disable the timing logic unit by setting the one or more bits in the control register of the timing logic unit to a second logic level different from the first logic level; and

repeat the first program instructions by decrementing or incrementing a predetermined expiration value, which is stored within a time register of the timing logic unit, by the number of pulses generated during each repetition of the first program instructions, such that the first program instructions are repeated a number of times equal to the predetermined expiration value divided by the number of pulses generated per repetition.

34. The computer-usable carrier medium as recited in claim 33, wherein the computer-usable carrier medium comprises one or more buses within the computer system.

35. The computer-usable carrier medium as recited in claim 33, wherein the computer-usable carrier medium comprises a wired or wireless network interface for coupling the computer system to one or more additional computer systems.

36. The computer-usable carrier medium as recited in claim 33, wherein the computer-usable carrier medium comprises a memory device within the computer system.